Paper No. 31

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte RAHUL RAZDAN,
JAMES B. KELLER
AND
RICHARD E. KESSLER

_____

Appeal No. 2002-2309
Application 09/099,386

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ON BRIEF

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Before HAIRSTON, BARRETT, and GROSS, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 1 through 24.

The disclosed invention relates to a method and system for maintaining cache coherence in a multiprocessor system that has a plurality of caches and a main memory.

Claims 1 and 12 are illustrative of the claimed invention, and they read as follows:

1. A system for managing access to caches connected to a plurality of processors in a multiprocessor system, comprising:

a system port connectable to each of the plurality of processors and configured to receive a request from a first one of the processors, the request asking to modify a block of a first cache of the caches, and the request corresponding to a coherence state of the block of the first cache;

a memory manager connected to the system port and configured, in response to the received request, (i) to direct sending, over the system port, of probes to the caches, other than the first cache, (ii) to receive cache state information, over the system port, responsive to the probes, (iii) to determine an acknowledgment based on the received cache state information representing one of permission granted and permission denied to modify the block of the first cache, and (iv) to direct sending, over the system port, of the acknowledgment, to the first one of the processors; and

wherein the memory manager does not internally duplicate a coherence state of blocks of the caches.

12. A method of maintaining cache coherence in a multiprocessor system having a plurality of caches and a main memory, comprising the steps of:

sending a request to modify a block of a first cache of the plurality of caches, the request corresponding to a coherence state of the block of the first cache;

sending probes to the caches, other than the first cache, to receive cache coherence state information responsive to the probes, said probes each contain at least a data movement field and a next state field;

determining an acknowledgment based on the received cache coherence state information representing one of permission

granted and permission denied to modify the block of the first cache; and

sending the acknowledgment to the first cache.

The references relied on by the examiner are:

Galles et al. (Galles)	5,504,874	Apr. 2, 1996
Nishtala et al. (Nishtala)	5,634,068	May 27, 1997

Claims 1 through 11 and 24 stand rejected under the first paragraph of 35 U.S.C. § 112 for lack of written description. According to the examiner (answer, page 3) "[t]here is no recitation in the specification, of any use (or even non-use) of duplicate coherence states, as set forth in the newly added claim limitations."

Claims 1 through 24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nishtala in view of Galles.

Reference is made to the brief (paper number 27) and the answer (paper number 28) for the respective positions of the appellants and the examiner.

OPINION

We have carefully considered the entire record before us, and we will sustain the lack of written description rejection of claims 1 through 11 and 24, and we will reverse the obviousness rejection of claims 1 through 24.

Appellants argue (brief, pages 7 through 11) that the prior art (U.S. Patent No. 5,634,068 to Nishtala) discloses a memory management system (i.e., a system controller 100) that uses "duplicate cache tags," that one of ordinary skill in the art would recognize that their specification describes a system where the memory management system need not maintain duplicate cache tags, and that the declaration submitted by Jeffrey C. Stevens demonstrates that the inventors were in possession of the idea of a cache controller system which does not need to duplicate the cache tags on the June 18, 1998 filing date of the application.

For an answer to appellants' arguments, we turn to In re Wohnsiedler, 315 F.2d 934, 937, 137 USPQ 336, 339 (CCPA 1963) which states:

> Though prior art may be used to show what matters would lie within the knowledge of one skilled in the art to explain ambiguities in an application, it cannot be used to supply specific limitations not found therein. The question is not what modification of appellants' disclosure might occur to one skilled in the art, it is rather whether the invention they are claiming is *described* in their specification.

The mere fact that appellants could have thought of the idea of a cache controller system that does not need to duplicate the cache tags on the filing date does not necessarily mean that they in fact invented such an idea on that date. The Stevens'

declaration (pages 2 and 3) states that the portion of the disclosure (specification, page 31) that states "[t]he memory management system may only have partial knowledge of the cache system states" provides written description support for the questioned claimed phrase "wherein the memory manager does not internally duplicate a coherence state of blocks of the caches." In response, the examiner contends (answer, page 14) that "the memory management system has some (partial) knowledge of the cache states" and that he "does not see how partial knowledge of the cache state could be considered as expressly stating not knowing the cache state." We agree with the examiner's contentions. The quoted portion of the specification does not state that the system has no knowledge of the cache states, and the "broad disclosure of 'alternate scenarios' does not provide sufficient support for the specific claim language regarding not using duplicate cache tags" (answer, page 14). The remainder of the Stevens' declaration presents nothing more than pure conjecture. Appellants ask the question (brief, page 12) "[i]f duplicate cache tags were used (such as in *Nishtala*), the specification would 'cry out' for a mention, yet no mention is made." We disagree. Notwithstanding the knowledge attributed to the skilled artisan, appellants must still describe in the

disclosure their contribution to the art pertaining to "duplicate cache tags" or the lack of such cache tags in the memory management system. Appellants' arguments (brief, page 8 and 9) to the contrary notwithstanding, the burden of proof properly shifted to appellants after the examiner successfully demonstrated that the noted claim limitation did not have any express written description support in the disclosure. Thus, we agree with the examiner's position (answer, pages 13 through 16) that neither appellants' arguments nor the Stevens' declaration proves that the memory management system does not internally duplicate "a coherence state of blocks of the cache," and the rejection of claims 1 through 11 and 24 is sustained because "the negative limitations recited in the present claims, which did not appear in the specification as filed, introduce new concepts and violate the description requirement of the first paragraph of 35 U.S.C. 112." Ex parte Grasselli, 231 USPQ 393, 394 (Bd. App. 1983), aff'd mem., 738 F.2d 453 (Fed. Cir. 1984).

Turning to the obviousness rejection of independent claims 1 through 24, the examiner has made extensive fact findings concerning the teachings of Nishtala (answer, pages 3 through 6), but the appellants only take issue (brief, pages 18 through 21) with the examiner's finding (answer, page 6) that "[i]t would

have been obvious to one of ordinary skill in the art, having the teachings of the Nishtala *et al*. before him at the time the invention was made, to modify the cache coherency system controller taught by the Nishtala *et al*., to incorporate the snoop architecture or memory directory architecture for maintaining cache coherency, as taught in the background of Nishtala *et al*., to maintain coherency by use of a directory by making cache state information available to the system processor in a memory directory architecture, in order to provide for a number of benefits, e.g., smaller chip size, as taught by Nishtala *et al*."

Appellants argue (brief, pages 19 and 20) that neither the cache snoop architecture nor the memory directory architecture teachings in the background of Nishtala mentions a memory manager, that it is improper to modify Nishtala's preferred embodiment that uses duplicate cache tags with the background teachings of this reference, and that the modified teachings of the reference still neither would teach nor would have suggested a memory manager that operates without duplicate cache tags.

We agree with appellants' arguments. Nothing in the record teaches or would have suggested the proposed modification of the teachings of Nishtala. Even if the teachings of Nishtala were

combined as suggested by the examiner, the skilled artisan would still not know from the combined teachings whether the memory manager in the preferred embodiment should not use duplicate cache tags. Any rejection put forth by the examiner must be supported by substantial evidence in the record, and, when that evidence is lacking in the record, the Board can not and should not resort to unsupported speculation to lend credence to the rejection. See In re Lee, 277 F.3d 1338, 1343, 61 USPQ2d 1430, 1433 (Fed. Cir. 2002), and In re Zurko, 111 F.3d 887, 889, 42 USPQ2d 1476, 1478-79 (Fed. Cir. 1997). The only teaching of record of a memory manger without duplicate cache tags is appellants' disclosed and claimed invention, and it is not available to the examiner in an obviousness rejection. Thus, the obviousness rejection of claims 1 through 11 and 24 is reversed.

With respect to claim 12, and the claims that depend therefrom, the examiner is of the opinion (answer, page 9) that the DTag New State Values 322 and the S_REPLY type 325 entries in the Status Vector in Active Transaction Status Array 294 in Figure 14 of Nishtala are a "data movement field" and a "next state field," respectively.

Appellants argue (brief, pages 22 and 23) that:

> The DTags of *Nishtala* are **duplicate cache tags** attached to *Nishtala's* system controller 110. *See Nishtala's* Figure 1. The fact that a **duplicate cache tag** needs updating is not related to a next state field of a probe command **sent to caches of processors** of a multiprocessor system. For this reason alone Applicants submit that the Examiner's logic is flawed and that the rejection should be reversed.
>
> The figures relied upon by the Examiner, as well as the corresponding portions of the specification do not teach, suggest or even imply, alone or in combination with *Galles*, that the probe command should have both a data movement field and a next state field. *Nishtala* discloses that the "System Controller 110 maintains a pending transaction status array 200 that stores information on all pending and Active transaction[s]." *Nishtala*, Col. 54, lines 6-8 . . . .
>
> Clearly, *Nishtala's* Transaction Status Array 200 is an array residing within the System Controller 110. In spite of this teaching, the Examiner relies upon particular entries in the Status Array 200, DTag state values 322 and S_REPLY type 325, for a teaching [of] a probe command having both a data movement field and a next state field . . . . *Nishtala*, however, does not teach, suggest or even imply that these two entries in the array should be sent together within a probe command to a processor. Further, since the DTags of *Nishtala* are part of the system controller, why would *Nishtala* teach that this entry should go anywhere beyond the system controller?

We agree with the appellants' arguments. Nothing in the record supports the examiner's contentions. For this reason, the obviousness rejection of claims 12 through 23 is reversed.

DECISION

The decision of the examiner rejecting claims 1 through 11 and 24 under the first paragraph of 35 U.S.C. § 112 is affirmed, and the decision of the examiner rejecting claims 1 through 24 under 35 U.S.C. § 103(a) is reversed. Accordingly, the decision of the examiner is affirmed-in-part.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

KENNETH W. HAIRSTON Administrative Patent Judge	)	
LEE E. BARRETT Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
ANITA PELLMAN GROSS Administrative Patent Judge	)	

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